REMARKS

Bearing in mind the comments in the Official Action, the application has been amended so as to place it in condition for allowance. An early indication of the same would be appreciated.

Claims 1-67 are now pending in this application. Claims 1, 37, and 51 are independent. Claims 1-7, 16, 25, 26, 35, 37, and 51 have been amended, and claims 55-67 have been added by this amendment. No new matter has been added by any claim amendment or new claim.

The Specification has been amended to correct several occurrences of "Fm" to read "μm". These typographical errors resulted from an erroneous conversion between word processing formats. No new matter has been entered by this amendment.

Withdrawal of the rejection of claims 2, 5, 16, 25, and 26 under 35 U.S.C. §112, second paragraph, as being indefinite, is requested. These claims have been amended in manner that is believed to remove the bases for indefiniteness.

As for the previous recitation of "about" objected to by the Examiner, the various claims have been amended to recite "approximately". "The use of the words 'substantially' and 'approximately' in a claim does not necessarily render it vague and therefore invalid under 35 U.S.C. §112."[1] As the Board of Patent Appeals and Interferences has stated, "[i]n rejecting the claim under the second paragraph of 35 U.S.C. § 112, it is incumbent on the Examiner to establish that one of ordinary skill in the pertinent art, when reading the claims in the light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity in the particular area as set out and circumscribed by the claims.[2] Applicants respectfully suggest that a person of ordinary skill in the art would not have been confused by the recitations of "about" or "approximately" in this art. Therefore, withdrawal of the indefiniteness rejections is requested.

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[1] *H.M. Chase Corp. v. Idaho Potato Processors, Inc.*, 185 U.S.P.Q. 106, 116 (Idaho 1974).
[2] *Ex Parte Wu*, 10 U.S.P.Q.2d 2031, 2033, (BPAI 1988).

Withdrawal of the rejection of claims 1, 2, 5-11, 13, 14, 16, 17, 20-27, 29-32, 34, 37, 39, 40, 43-49, and 51-54 under 35 U.S.C. §103(a) as being unpatentable over Duncan et al. (US 4,585,931) in view of Iwai (US 4,418,467) is requested.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim limitations***[3] (emphasis added). Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[4]

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.[5] Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[6]

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[7] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[8] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[9]

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[3] *See* MPEP §2143.
[4] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[5] *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)
[6] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)
[7] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[8] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).
[9] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).

Duncan et al. represents the conventional approach for identifying semiconductor wafers using bar code identification indicia, as discussed in the present Specification. Further, Duncan et al. is directed to a technique for solving a bar-code readability problem by widening the bar code aspect ratio. As also discussed at page 7 of the Specification, for example, bar codes on semiconductor wafers typically cannot be read after process steps have been completed, and use of bar codes for such semiconductor wafer identification is at least undesirable in this respect. Thus, Duncan et al. teaches away from at least one aspect of Applicants' invention, as recited in independent claims 1, 37, and 51, as amended. Further, Duncan et al. does not teach or suggest use of a digital information pattern, which is other than a bar code pattern.

Iwai is directed to a method for manufacturing a semiconductor device having alignment or information marks on a side surface thereof. Based upon the disclosure of Iwai, the information mark may be letters or numerals, or "other characters such as hiraganas, katakanas, and Greek letters, or symbols such as bar patterns."[10] Iwai does not teach or suggest use of a digital information pattern, which is other than a bar code pattern.

In particular, the applied art, either alone or in combination, does not teach or suggest a semiconductor wafer which includes, among other features, "a plurality of pits in the semiconductor wafer, the pits being arranged in a ***digital information-providing pattern other than a bar code pattern*** which is readable before, during and after completion of processing on the wafer", as recited in independent claim 1, as amended.

In addition, the applied art, either alone or in combination, does not teach or suggest a method of encoding information on a semiconductor wafer which includes, among other features, "converting the information ***into a digital form other that a bar code pattern***", as recited in independent claim 37, as amended.

Further, the applied art, either alone or in combination, does not teach or suggest a system for encoding information on a semiconductor wafer and reading the information, wherein the system includes, among other features, "a plurality of pits formed on the semiconductor wafer ***in***

[10] *See* Iwai (US 4,418,467), col. 7, lines 21-25.

a digital information-providing pattern other than a bar code pattern", as recited in independent claim 51, as amended.

Accordingly, reconsideration and allowance of independent claims 1, 37, and 51 are requested. Further, as dependent claims 2-36, 38-50, and 52-54 variously and ultimately depend from independent claims 1, 37, and 51 and, consequently, incorporate their allowable features, these dependent claims are also submitted as being allowable, without recourse to the additional patentable limitations respectively recited.

Withdrawal of the rejection of claims 3, 4, 48, and 50 under 35 U.S.C. §103(a) as being unpatentable over Duncan et al. and Iwai in view of Moh et al. (US 6,214,250) and Yano et al. (US 6,268,641) is requested. Even assuming that Moh et al. and Yano et al. are properly combinable with Duncan et al. and Iwai, Moh et al. and Yano et al. do not make up for the previously identified deficiencies of Duncan et al. and Iwai as discussed above with respect to independent claims 1 and 37. Therefore, reconsideration and allowance of claims 3, 4, 48, and 50 are requested.

Withdrawal of the rejection of claims 12, 18, 19, and 41 under 35 U.S.C. §103(a) as being unpatentable over Duncan et al. and Iwai in view of Young et al. (US 5,792,566) is requested.

Young et al. is directed to improved commercial single crystal wafers, which have a stress concentration notch that allows cleaving the crystal along a desired cleavage plane. Notch 172, offered by the Official Action as disclosing "the pit", is actually a stress concentration notch formed by longitudinal cut 171. Notch 172 facilitates cleavage of the crystal wafer by concentration of the cleaving forces applied at or near the score line. Applicants submit that Young et al. is directed to the solution of a completely different technical problem, and is therefore submitted as not being properly combinable with Duncan et al. and Iwai.

Even assuming that Young et al. is properly combinable with Duncan et al. and Iwai, which Applicants do not admit, Young et al. do not make up for the previously identified deficiencies of Duncan et al. and Iwai as discussed above with respect to independent claims 1 and 37. Therefore, reconsideration and allowance of claims 12, 18, 19, and 41 are requested.

Withdrawal of the rejection of claims 15, 36, and 42 under 35 U.S.C. §103(a) as being unpatentable over Duncan et al. and Iwai in view of Yagi et al. (US 5,324,609) is requested.

Yagi et al. is offered as teaching the coating of the surface of the wafer with silicon carbide. While this may be true, dependent claim 15 recites that the wafer comprises a coating on the surface of the pits, not on the surface of the wafer, and method claim 42 recites a step of coating the pits with a coating.

As for the motivation to combine Duncan et al. and Iwai with Yagi et al. in the manner suggested by the Examiner, Applicants submit that the Official Action has not established the proper motivation to combine the references. Yagi et al. is directed to a Carlson system electrophotographic photoreceptor having a small dark current decay and improved mechanical strength, and which finds application in a laser printer, for example.

The Official Action indicates that Yagi et al. discloses coating the surface of the wafer with silicon carbide, but broadly points to col. 5, line 51 through col. 9, line 54, and does not cite the asserted teaching with precision. The portion of Yagi et al. referenced by the Examiner merely teaches how to build the photoreceptor. However, Yagi et al. at col. 7, lines 4-14 does disclose that amorphous silicon carbide may be used to form an intermediate layer between the surface layer and photoconductive layer to lessen the influences of surface oxidation on the surface layer, and also to block charge injection from the surface layer.

Whether or not Yagi et al. teaches or suggests coating a surface of the wafer with silicon carbide, it is clear that Yagi et al. does not teach or suggest a plurality of pits in the semiconductor wafer arranged in a digital information-providing pattern, and still further does not teach or suggest that a surface of the pits are coated with, for example, silicon carbide.

Further, the Official Action goes on to state that "[i]t would have been obvious to a person having skill in the art...to incorporate the teachings [of] Yagi to the teachings of Duncan/Iwai in order to prevent/reduce the wear-off and tear-off of the surface of the wafer by coating the surface

of the wafer. Moreover, such modification would provide the clear reading of the pits since the coating of the wafer surface prevent[s] dust materials from resting within the pits, and therefore [is] an obvious expedient." Applicants respectfully traverse this assertion.

Applicants submit that a person having skill in the art would not be motivated to combine Yagi et al. with Duncan et al. and Iwai, as Yagi et al. is directed to the solution of a completely different technical problem than the recited invention. Even assuming, *arguendo*, that the references are properly combinable as suggested by the Examiner, the applied art, taken alone or in combination, does not teach or suggest all the claim limitations of independent claims 1 and 37, from which claims 15 and 42 respectively depend.

Applicants point out that it is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art.[11] Further in this regard, As the Court of Customs and Patent Appeals, predecessor to the Federal Circuit, has held:

> All relevant teachings of cited references must be considered in determining what they fairly teach to one having ordinary skill in the art. The relevant portions of a reference include not only those teachings which would suggest particular aspects of an invention to one having ordinary skill in the art, but also those teachings which would lead such a person away from the claimed invention.[12]

The rejection of claim 15 in the Official Action amounts, in substance, to nothing more than hindsight reconstruction of Applicants' invention, by relying on isolated teachings of the applied art, without considering the overall context within which those teachings are presented. Without benefit of Applicants' disclosure, a person having ordinary skill in the art would not know what portions of [Duncan et al., Iwai, and Yagi et al.] to consider, and what portions to disregard as irrelevant or misleading.[13] The Official Action overreaches by asserting that the

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[11] *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986).
[12] *In re Mercier*, 185 USPQ 774, 778 (CCPA 1975).
[13] *In re Wesslau*, 147 USPQ 391, 393 (CCPA 1965).

mere disclosure of an amorphous layer of silicon carbide discloses the dependent claim features discussed above.

Accordingly, reconsideration and allowance of claims 15, 36, and 42 are requested.

Withdrawal of the rejection of claim 28 under 35 U.S.C. §103(a) as being unpatentable over Duncan et al. and Iwai in view of Mitsuda et al. (US 5,481,095) is requested.

Mitsuda et al. is directed to a code reading pattern and image pickup apparatus which is adapted to read a code reading pattern formed by repeated markings of constant pitch on the surface of an object.

As discussed above, Duncan et al. and Iwai are directed to wafers having a bar code pattern. Applicants submit that a bar code pattern is not formed by "repeated markings of constant pitch on the surface of an object", and that Mitsuda et al. is therefore, not combinable at least with Duncan et al.

Even assuming that the references are properly combinable as suggested by the Examiner, Mitsuda et al. does not make up for the previously identified deficiencies of Duncan et al. and Iwai, as discussed above with respect to independent claim 1. Therefore, reconsideration and allowance of claim 28 are requested.

Withdrawal of the rejection of claims 33, 35, and 38 under 35 U.S.C. §103(a) as being unpatentable over Duncan et al. and Iwai in view of Fujita et al. (US 6,293,466) is requested.

Fujita et al. is directed to a bar code image processing apparatus, which uses a bar code having bars with the same width and different lengths. Independent claims 1 and 37, from which claims 33 and 35, and 38 respectively depend, claim "a plurality of pits in the semiconductor wafer, the pits being arranged in a digital information-providing pattern ***other than a bar code pattern***" (emphasis added), as recited in independent claim 1, and "converting the information

into a digital form ***other that a bar code pattern***" (emphasis added), as recited in independent claim 37, as amended.

Therefore, Applicants submit that Fujita et al. teaches away from at least one aspect of the recited invention, as amended. Further, Fujita et al. does not make up for the previously identified deficiencies of Duncan et al. and Iwai, as discussed with respect to independent claims 1 and 37. Accordingly, reconsideration and allowance of claims 33, 35, and 38 are requested.

Newly presented dependent claims 55-6XXX have been drafted to avoid the cited art and the rejections for indefiniteness, and are submitted as being patentable at least on the basis of the various independent claims from which they depend, as well as in their own right. No new matter has been entered by these claims.

For example, dependent claim 55 recites a semiconductor wafer wherein the plurality of pits are simultaneously arranged in both a digital information-providing pattern and a human-readable pattern, as illustrated, for example, in Fig. 12. None of the applied or cited art teaches or suggests this feature.

As a further example, dependent claim 56 recites a semiconductor wafer wherein the digital information-providing pattern is a non-binary coded pattern, and the plurality of pits comprise pits having at least three different shapes, as discussed at least at the bottom of page 11 and top of page 12 of the Specification.

As yet another example, dependent claim 58 recites a semiconductor wafer wherein the digital information-providing pattern is a non-binary coded pattern, and the plurality of pits comprise a plurality of differently oriented oval pits as defined by an orientation of each of an associated major axis thereof, for which general disclosure may be found at least at page 11, lines 14-19 of the Specification.

Consideration and allowance of new dependent claims 55-67 are therefore requested.

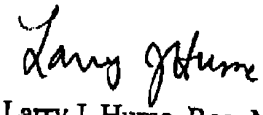
In view of the above, consideration and allowance of pending claims 1-67 are, therefore, respectfully solicited.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below. Further, in the event that a Notice of Allowance is not forthcoming in response to this Amendment, the undersigned requests that a personal interview be granted with the Supervisory and Assistant Examiners in this case.

Pursuant to 37 C.F.R. §§1.17 and 1.136(a), Applicant hereby petitions for an extension of time for one (1) month to May 30, 2002 for filing a reply to the final Office Action dated January 30, 2002 in connection with this application. The petition and deposit account authorization for CBLH Deposit Account No. 22-0185 is enclosed herewith.

Fees for excess claims are to be charged to IBM Deposit Account No. 09-0456.

Respectfully submitted,



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Enclosure: Specification after Amendment
Claims after Amendment
Petition for one (1) month extension of time
Transmittal sheet for excess claims

Specification after Amendment

IN THE SPECIFICATION:

Please amend the Specification as follows:

Please replace the paragraph at line 18, page 12 of the Specification with the following replacement paragraph:

--Similarly, the depth of the pits may depend upon where they are formed. Pits formed on an edge of a semiconductor wafer may be formed a much greater distance into the material of the semiconductor wafer than pits formed on a front or back surface of the semiconductor wafer. Pits formed on a front or back surface of a semiconductor wafer may be formed a depth of at least about 2.5 ~~Fm~~ µm into the material of the semiconductor wafer.--

Please replace the paragraph at line 4, page 13 of the Specification with the following replacement paragraph:

--As with the other dimensions, the spacing between pits may vary depending upon the embodiment. According to one embodiment, pits are separated from each other by distance of about 2 millimeters. Typically this is the case for pits formed in an edge of a semiconductor wafer. Pits formed in front or back surface of the semiconductor wafer may be arranged much closer to each other. Along these lines, the pits may be formed separated from adjacent pits by a distance by about 5 ~~Fm~~ µm to about 10 ~~Fm~~µm. According to one embodiment a distance of at least about 5 ~~Fm~~ µm separates adjacent pits in a line or adjacent lines from each other.--

Please replace the paragraph at line 15, page 30 of the Specification with the following replacement paragraph:

--Similar to the characters and the spacing between the characters, the pits making up the characters may be formed in different sizes, shapes, and depth, among other parameters. Typically, the pits are round, have a diameter of about 0.6 ~~Fm~~ µm to about 1.0 ~~Fm~~ µm and a

depth of about 25 ~~Fm~~ μm to about 100 ~~Fm~~ μm and are spaced about 0.3 ~~Fm~~ μm to about 0.6 ~~Fm~~ μm from adjacent pits.--

Please replace the two paragraphs starting at line 12, page 32 of the Specification with the following replacement paragraphs:

--Fig. 10 provides a close-up partial cross-sectional view through three pits formed on a surface of a semiconductor wafer. The pits 52 formed in semiconductor wafer 50 are each about 50 ~~Fm~~ μm wide.

The pits illustrated in Fig. 10 are formed to have straight sidewall portions about 5 ~~Fm~~ μm deep. Each pit also includes a rounded bottom portion 68. Forming the pits about 5 ~~Fm~~ μm deep is deep enough to stop subsequent processes from obscuring the pits. Of course, pits may be formed having a depth and diameter as well as having any configuration of sidewalls and bottom surfaces.--

Please replace the paragraph starting at line 1, page 33 of the Specification with the following replacement paragraph:

--Approximately the top 5 ~~Fm~~ μm 54 of semiconductor wafer 50 represent an area where the ion implant has been carried out. According to this embodiment, the ion implant changes the index of refraction of this top of about 0.5 ~~Fm~~ μm on the surface. The change to the index of refraction is illustrated by incident radiation beam 56 and the refraction illustrated by beams 58. The radiation is then reflected by the non-implanted portion of the semiconductor wafer as illustrated by beams 60. Fig. 3 also provides a representation a waveform of the radiation 62.--

Please replace the paragraph starting at line 17, page 33 and ending on line 1, page 34 of the Specification with the following replacement paragraph:

--As illustrated in Fig. 12, pits may be formed in a semiconductor wafer in groups forming alphanumeric characters. Fig. 12 illustrates two characters. Each character is about 5

mm long by about 2 mm wide. Such characters would be about 50 dots having a length of about 50 ~~Fm~~ µm by about 20 dots having a length of about 50 ~~Fm~~µm. Such characters would give a resolution of 2500 dots per inch (DPI). Such characters are more than large enough to make the characters readable by the naked eye.--

Please replace the three paragraphs starting at line 1, page 37 of the Specification with the following replacement paragraphs:

--Fig. 16 represents a close-up cross-sectional view of the group of pits illustrated in Fig. 15 along the line 16 illustrated in Fig. 15. The pits illustrated in Fig. 16 have a width W of about 0.4 ~~Fm~~ µm and a depth (D) of about 2 ~~Fm~~ µm and are spaced apart a distance (S) of about 0.75 ~~Fm~~µm.

While pits according to the embodiment illustrated in Figs. 13-16 may be formed at any depth, typically, the depth is sufficient to ensure that the pits remain readable during subsequent processing as well as to help ensure contrast with any treatment carried out on the backside of the wafer. Typically, the pits are formed at least 2.5 ~~Fm~~ µm deep into a surface of a semiconductor wafer. In general, the pits may be about 1.5 ~~Fm~~ µm to about 3 ~~Fm~~ µm deep.

The spacing between adjacent pits and between adjacent rows of pits may also vary. Along these lines, adjacent pits typically are spaced about 0.5 ~~Fm~~ µm to about 1 ~~Fm~~ µm apart. On the other hand, adjacent rows of pits typically are spaced about 0.5 ~~Fm~~ µm to about 2.0 ~~Fm~~ µm apart.--

Please replace the paragraph starting at line 3, page 38 of the Specification with the following replacement paragraph:

--In the embodiment shown in Figs. 13-16, if 50 ~~Fm~~ µm were required to encode an alphanumeric character, 50 characters could be encoded in a line about 2.5 millimeters. Therefore, the embodiment illustrated in Figs. 13-16 can make it easy to encode wafer serial

numbers, substrate type, doping level, manufacture, among other pieces of information. Such data could be encoded in the pits utilizing a laser, ion milling, or mask and etch procedures.--

Claims after Amendment

IN THE CLAIMS:

Please amend claims 1-7, 16, 25, 26, 35, 37, and 51 as follows:

1. (Amended) A semiconductor wafer, comprising:

a plurality of pits in the semiconductor wafer, the pits being arranged in ~~an~~ a digital information-providing pattern other than a bar code pattern which is ~~and being~~ readable before, during and after completion of processing on the wafer.

2. (Amended) The wafer according to claim 1, wherein ~~the~~ a readability of the pits is provided by the pits having ~~sufficient~~ a detectable contrast with respect to surrounding portions of the wafer.

3. (Amended) The wafer according to claim 2, wherein the pits are arranged in a region of the wafer, wherein the contrast is provided by an ion implant in the region.

4. (Amended) The wafer according to claim 3, wherein the ion implant is carried out to ~~a~~ an implant depth and the pits have a pit depth greater than the ~~ion~~ implant depth.

5. (Amended) The wafer according to claim 2, wherein the pits are arranged in a region of the wafer, wherein the detectable contrast is provided by a depth of the pits ~~having a sufficient depth~~.

6. (Amended) The wafer according to claim 1, wherein the digital information providing pattern comprises at least one of a ~~bar code, a digital pattern, a~~ binary pattern, ~~or~~ and an alphanumeric pattern.

7. (Amended) The wafer according to claim 61, wherein the digital pattern comprises long and short pits.

16. (Amended) The wafer according to claim 1, wherein the pits have a width of at most ~~about~~ approximately 1 mm and a depth of at most ~~about~~ approximately 1 mm.

25. (Amended) The wafer according to claim 24, wherein each group of pits has a width of ~~about~~ approximately 2 mm and a height of ~~about~~ approximately 5 mm.

26. (Amended) The wafer according to claim 24, wherein adjacent groups of pits are separated from each other by a distance of ~~about~~ approximately 2 mm.

35. (Amended) The wafer according to claim 33, wherein adjacent pits in a line or in adjacent lines are separated by a distance of at least 5 ~~Fm~~μm.

37. (Amended) A method of encoding information on a semiconductor wafer, comprising:

converting the information into a digital form other that a bar code pattern; and

forming pits readable before, during and after completion of processing on the wafer corresponding to the digital form of the information in the semiconductor wafer.

51. (Amended) A system for encoding information on a semiconductor wafer and reading the information, the system comprising:

a plurality of pits formed on the semiconductor wafer in ~~an~~ a digital information-providing pattern other than a bar code pattern,

wherein the digital information-providing pattern ~~and being~~ is readable before, during and after completion of processing on the wafer; and

means for reading the information encoded by the pits.